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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,002	12/09/2003	Raymond Jit-Hung Sung	9-16319-251US	2813

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,002	SUNG ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12-9-2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because lines, numbers & letters in Figs. 1 - 28 are not uniformly thick and well defined, clean, durable, and black and letters are overlapped with lines. 37 CFR 1.84(l). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 3-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakajima (US PAT No. 3,999,081).

Regarding claim 1, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches a single-rail multi-gate domino logic circuit (Figs. 1a-1f, 3a1-3f1 connected in series according to Figs. 5a - 5c; col. 2, lines 28-30) driven by a multi-phase clock (Φ1, Φ2, Φ3) comprising: a first dynamic logic gate (Fig. 1d or Fig. 3a1) having an evaluate clock logic circuit (70 in Fig. 1d, 20 and 54 in Fig. 3a1) comprising at least first and second transistors (71,72 in Fig. 1d, 20 and 54 in Fig. 3a1) driven by respective separate phases of the multi-phase clock.

Regarding claim 3, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches the domino logic circuit as claimed in claim 1 wherein the first and second transistors are connected to perform any one of: a logical OR-function of a current clock phase and a next clock phase (when both of Φ1 & Φ2 are low, the output is low in Fig. 1d); a logical AND-function of a current clock phase and a previous clock phase.

Regarding claim 4, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches the domino logic circuit as claimed in claim 1 wherein the dynamic logic stage further comprises a precharge clock logic circuit (53 in Fig. 3a1) having at least first and second transistors (51 & 52) driven by respective separate phases of the multi-phase clock signals (Φ1, Φ2).

Regarding claim 5, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches the domino logic circuit as claimed in claim 1 wherein the first dynamic logic gate comprises any one of: an input complemented logic gate (Fig. 3a1 is a standard dynamic logic inverter); a non-monotonic logic gate; and a standard dynamic logic gate.

Regarding claim 6, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches the domino logic circuit as claimed in claim 5, further comprising a plurality of logic phases connected in series, each logic phase comprising a respective first logic gate (Figs. 1a-1f, 3a1-3f1 connected in series according to Figs. 5a - 5c; col. 2, lines 28-30, e.g. Fig. 3a1 may be coupled to any of Fig. 3b1 - 3f1) .

Regarding claim 7, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches the domino logic circuit as claimed in claim 6, wherein at least one logic phase further comprises a second logic gate connected in series with the respective first dynamic logic gate (Figs. 1a-1f, 3a1-3f1 connected in series according to Figs. 5a - 5c; col. 2, lines 28-30, e.g. Fig. 3a1 may be coupled to any of Fig. 3b1 - 3f1).

Regarding claim 8, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches the domino logic circuit as claimed in claim 7, wherein the second logic gate comprises either one of: a static logic gate; and a standard dynamic logic gate (Figs. 3b1 - 3f1 are a standard dynamic logic gate).

Regarding claim 9, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches a single-rail domino circuit (Figs. 1a-1f, 3a1-3f1) driven in accordance with a multi-phase clock (Φ1, Φ2, Φ3), comprising: a plurality of logic phases connected in series (Figs. 1a-1f, 3a1-3f1 connected in series according to Figs. 5a - 5c; col. 2, lines 28-30), each logic phase being associated with a respective current clock phase (Φ1, Φ2, Φ3), and comprising at least one dynamic logic gate (Figs. 1a-1f, 3a1-3f1 are dynamic logic gate); a respective evaluate clock logic circuit (70 in Fig. 1d, 60 in Fig. 1b) connected to control an evaluate cycle of each dynamic logic gate, the evaluate clock logic circuit comprising respective first and second transistors connected to receive the respective current clock phase (Φ1 in Fig. 1d, Φ3 in Fig. 1b) and an adjacent clock phase (Φ2 in Fig. 1d, Φ1 in

Fig. 1b), such that overlap between a precharge cycle of a first logic phase and an evaluation cycle of an adjacent logic phase is prevented (Fig. 4).

Regarding claim 10, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches a single-rail domino circuit as claimed in claim 9, wherein a first dynamic logic gate lies on a boundary between its respective logic phase and a previous logic phase (Figs. 1a-1f, 3a1-3f1 connected in series according to Figs. 5a - 5c; col. 2, lines 28-30, e.g. Fig. 3a1 may be coupled to any of Fig. 3b1 - 3f1), and comprises any one of: an input complemented logic gate (Fig. 3a1 is a complementary, i.e. inverter dynamic logic gate); a non-monotonic logic gate; and a standard dynamic logic gate.

Regarding claim 11, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches a single-rail domino circuit as claimed in claim 10 wherein the first dynamic logic gate is connected in series with a second logic gate (Figs. 1a-1f, 3a1-3f1 connected in series according to Figs. 5a - 5c; col. 2, lines 28-30, e.g. Fig. 3a1 may be coupled to any of Fig. 3b1 - 3f1) within the same logic phase (Φ1, Φ2, Φ3 in Fig. 4), the second logic gate comprising either one of: a static logic gate; and a standard dynamic logic gate (Fig. 3a1 is a complementary, i.e. inverter dynamic logic gate).

Regarding claim 12, Figs. 1a-1f, 3a1 - 3f1 and 5a - 5c teaches a single-rail domino circuit as claimed in claim 9, wherein the first and second transistors are connected to perform any one of: a logical OR-function of the respective current clock

phase and a next clock phase (60 in Fig. 1b performs a logic OR function of Φ1, Φ3); a logical AND-function of the respective current clock phase and a previous clock phase.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima applied to claim 1 above, and further in view of Kumar (US PAT No. 5,426,383).

Regarding claim 2, Figs. 1a-f and 5a teaches the domino logic circuit as claimed in claim 1 wherein the transistors comprise p-type MOS FETs (71 and 72 in Fig. 1d) , but does not teach n-type MOS FETs.

However, Fig. 10A and Fig. 10C of Kumar teaches a PMOS (25 in Fig. 10A) is replaced with an inverter and NMOS (53 and 56 in Fig. 10C) for the purpose of providing faster speed (col. 7, line 56+).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to replace a PMOS of Nakajima with a NMOS and an inverter of Kumar or vice versa for the purpose of variation in speed.

Furthermore as a matter of engineering choice, it is well known in the art that a NMOS with the equivalent channel size as a PMOS provides higher driving current, so that it switches faster while a PMOS provides lesser threshold voltage.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Abdel-Haffez et al. (US PAT No. 6,265,899) discloses a single rail domino logic for four-phase clocking scheme.

Low et al. (US PAT No. 3,857,045) discloses four-phase logic system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

7-6-2005